Claim 1(twice amended). A test configuration, comprising:

a semiconductor wafer;

B1 a plurality of semiconductor chips disposed on said semiconductor wafer, each of said plurality of semiconductor chips having a self-test unit generating test information for functionally checking said semiconductor chip; and

an energy source disposed on said semiconductor wafer and connected to said semiconductor chip for providing an electrical energy supply to said semiconductor chip, said energy source having at least one solar cell for generating an operating current for said semiconductor chip by optical radiation fed in contactlessly, said solar cell being disposed on a surface of said semiconductor wafer remote from said semiconductor chip;

said semiconductor wafer having an electrically conductive plated-through hole formed therein disposed between said solar cell and said semiconductor chip, at a boundary between said plated-through hole and said semiconductor wafer, and said semiconductor wafer having a pn junction disposed along said plated-through hole for preventing a current flow between said plated-through hole and a remainder of said semiconductor wafer.

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Claim 7(amended). The test configuration according to claim 20, including a radiation-absorbing layer disposed between said solar cell and said semiconductor chip.

Claim 20(amended). A test configuration, comprising:

a semiconductor wafer having a surface with an area;

B3

a plurality of semiconductor chips disposed on said surface of said semiconductor wafer, each of said semiconductor chips having a self-test unit generating test information for functionally checking said semiconductor chip; and

an energy source disposed above said semiconductor wafer and connected to said semiconductor chip for providing an electrical energy supply to said semiconductor chip, said energy source having at least one solar cell for generating an operating current for said semiconductor chip by optical radiation fed in contactlessly, said solar cell being disposed areally entirely over said area of said surface of said semiconductor wafer.

Add the following claims:

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Claim 21. The test configuration according to claim 20, including a radiation-absorbing layer between said solar cell

and said semiconductor wafer, said radiation-absorbing layer having an electrically conductive plated-through hole formed therein disposed between said solar cell and said semiconductor chip.

Claim 22. The test configuration according to claim 21, wherein said radiation-absorbing layer has a pn junction disposed along said plated-through hole at a boundary between said plated-through hole and said radiation-absorbing layer for preventing a current flow between said plated-through hole and a remainder of said radiation-absorbing layer.